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Electronic device, assembly and methods of manufacturing an electronic device

The invention relates to an electronic device comprising a semiconductor substrate having a first and a second side and provided with a capacitor and a vertical interconnect through the substrate extending from the first to the second side, at which first side the capacitor is present.

The invention also relates to an assembly therewith.

The invention further relates to methods of manufacturing such an electronic device.

Such an electronic device is known from EP-A 1154481. The known device is an interposer that is made of a heat-resistant insulator, that is preferably silicon, but alternatively of glass or resin. Through-holes are made with a laser. Wiring patterns are then formed on both the first side and the second side of the device, said wiring pattern extending at the side walls of the through-holes and thus forming the vertical interconnect. Gold or solder bumps may be applied at the second side for connection to a mounting board. A capacitor is present at the first side of the substrate. The capacitor is a thin-film capacitor with a dielectric sandwiched between a first and second electrode. The first electrode forms herein part of the wiring pattern. The dielectric layer is formed preferably of a ferroelectric substance, such as strontium titanium oxide or lead zirconium titanate. Thus, a capacitor having a high capacitance density is obtainable.

It is however a disadvantage of the known device, that application of ferroelectric substances sets further conditions and requirements to the processing. Generally, specific metal layers such as platinum or a conductive oxide, are applied as electrode material for capacitors with such ferroelectric substances. An alternative appears the provision of an aftertreatment in reducing atmosphere after the provision and sintering of the ferroelectric substance. This aftertreatment at a high temperature is however not yet fully developed and has the problem that all layers in the device must be able to withstand the applied temperature and conditions. Furthermore, the ferroelectric substances are sensitive to delamination and

cracking, which is certainly the case if the first bottom electrode forms part of the wiring pattern and can thus be expected to have a relatively rough surface.

It is therefore an object of the invention to provide an electronic device of the kind mentioned in the opening paragraph, which combines the electrical connection through the substrate with the presence of capacitors with a high capacitance density and which is reliable and manufacturable.

This object is achieved in the invention in that the capacitor is a vertical trench capacitor provided with a plurality of trenches in which a layer of dielectric material is present between a first and a second conductive surface, said layer of dielectric material is also being used as isolation between the substrate and the vertical interconnect.

Vertical capacitors are alternatives to ferroelectric capacitors for providing a high capacity. The high capacity is herein achieved with an increase of the surface area. They are known per se, such as for instance from US-A 4,017,885. However, vertical capacitors cannot be substituted for ferroelectric capacitors directly. The same process is needed for making the through-holes and making the trenches of the vertical capacitors, but with different parameter settings. Hence, the manufacture of the trench capacitors and the vertical interconnects cannot be combined, but should be done subsequently.

This subsequent processing appears problematic as well, since the vertical interconnect must be isolated from the substrate adequately. If first the vertical capacitor is made, and then the interconnect, the capacitor and other layers made must be protected very well against the etching liquid or etching gas. The etching liquid or gas may easily open the interface between the substrate and the patterned layers and therewith lead to contamination, delamination and other undesired effects. The reverse order of making first the vertical interconnect and then the trench appears not available either. Not only will a large part of deposited material be removed through the vertical interconnect, but also an implantation step is required for the provision of a conductive surface in the vertical capacitor, which would be detrimental for the constitution of the vertical interconnect.

It is now the insight of the invention, that both the vertical capacitors and the vertical interconnects can be combined with good results, by using the dielectric material of the trenches also as the insulating material for the vertical interconnect. Both vertical elements are thus processed simultaneously, with steps done not only at the first side of the substrate, but also at the second side.

The resulting device has substantial advantages over the prior art; first of all, it is assured that it has adequate high-frequency properties. Due to the insulating material parasitic currents through the substrate are prevented, at least to a large extent. This insulating material can be effectively deposited, without a mask and including a thermal oxide layer.

Due to the presence of the vertical interconnects, it is possible to provide very short connections to ground. Short connections to ground are important for RF applications, as the ground is the reference. If due to impedances of interconnects the ground is not adequately grounded, the complete RF design may function detrimentally. Furthermore, short connections for signal lines reduce the impedances. This is particularly true, since the signal lines are not only shorter, but can be provided at locations so as to minimize parasitic behaviour or to establish microstrip behaviour.

Moreover, the high capacity capacitors can be used as decoupling capacitors for any integrated circuit to be applied at the first side. This will reduce the needed number of external contacts dramatically. Finally, the capacitor of the invention has a low resistance as compared to planar capacitors, which is particularly true for larger capacitance values of 20 nF and more, and especially for capacitors of more than 40 nF or more.

Besides, it is advantageous that one or more capacitors in the device of the invention can be used for more applications. Ferroelectric capacitors such as strontium titanium oxide show a dielectric adsorption. As a result of hereof open loop tranceivers with such capacitors for the PLL function do not give the required performance. Capacitors with another dielectric, such as silicon nitride or silicon oxide do not have this problem. Additionaly, the temparature stability of the dielectric constant of thin-film ferroelectric layers as far as currently available is less than optimal for applications in or together with transceivers.

It is another advantage of the device of the present invention as compared to that in the prior art, that it enables the provision of any desired capacitance value. If a larger capacitance value is needed, the capacitor will comprise a larger number of vertical trenches. Since the surface area on top of the vertical capacitors can be used for interconnects, resistors, inductors and the like, the larger capacitor does not give rise to a new design. Also, it is quite easy to provide capacitors with slightly different values while standard design rules can be respected.

In a preferred embodiment, the trenches of the interconnect are substantially filled with electrically conductive material. This filling of the trenches leads to a further

reduction of the impedance of the vertical interconnect. It is noted that such filling is not foreseen in the prior art EP-A 1154481. The reason thereof must be found in the actual diameter of the through-holes. Although the trenches of the interconnects are generally wider than those of the capacitors, the etching technique in which they are made allows relatively small diameters. With such small diameters the conductive material will first cover side walls but thereafter fill the trench. Moreover, the manufacture of the vertical interconnect generally occurs in a two step process, wherein first from the one side is etched and thereafter the trenches are opened from the opposite side. This manufacturing technique allows that the via is already filled halfway, before its opened.

In an even further embodiment, the vertical interconnect comprises a plurality of parallel through-holes through the substrate, each of which is filled with electrically conductive material. This construction allows the provision of a very low impedance. Not only does the resistance decrease due to the parallel circuitry, but also are circular currents within the vertical interconnect minimized, that would otherwise give rise to parasitic inductance. Another advantage is that the filling material may be the same as that of the second conductive surface of the capacitor. This reduces the number of process steps. A suitable filling material is polycrystalline silicon, doped with a conventional dopant.

In another suitable embodiment, a first vertical interconnect is used for grounding and a second interconnect is used for signal transmission. Grounding and signal transmission are important aspects of the function of an interposing substrate, if the device is used for RF applications. With the vertical interconnects, these functions can be fulfilled excellently.

In a further embodiment, the first and second vertical interconnect are designed so as to form a coaxial structure. The coaxial structure is one example of a microstrip. Such microstrips allow signal transmission with very limited impedance. Since the vertical interconnects are filled, contact pads may be provided at the second side of the substrate at the end of the vertical interconnects. Solder balls can be provided on such contact pads for connection to a printed circuit board. At the first side, the substrate is generally covered with an interconnect structure of a couple of layers. This allows that each of the vertical interconnects can be contacted without short-circuitry. Also, the coaxial structure may be transformed in the interconnect structure to any other type of a microstrip, such as a transmission line or a coplanar wave guide. Aims of the interconnect structure is not only the contacting of the capacitors and any resistor and/or inductor present, but also the rerouting of the signal path, so as to fit to the bumps of an integrated circuit.

In another embodiment an integrated circuit is defined at the second side of the substrate. This option allows a further integration of functionality. The contact pads of the device will then be provided at the first side of the substrate, adjacent and/or on top of the vertical capacitors. This embodiment appears particularly suitable for the application in smartcards. The advantage of this concept is that very large decoupling capacitors can be provided at the same substrate as the integrated circuit, without the requirement of additional space. Such a decoupling capacitor is part of the internal power supply circuit. The capacitor allows decoupling of the smartcard of any external power supply during a certain decoupling period. The decoupling period is then used for carrying out security-relevant operations. The very large decoupling capacitor thus allows that the decoupling period is extended, while at the same time no further surface area is needed. This construction of the decoupling capacitor is moreover advantageous from the perspective of security. In the current situation, both the capacitor and any data processing section are at the outer side of the smart card IC, and hence vulnerable to attack and misuse by unauthorized persons. By replacing the capacitor to the other side, only one of both sides is present at the outer side. In a further embodiment, the device further comprises a scratch-protective, non-transparent layer. Such a layer, also called 'security coating' is specifically aimed at preventing access to the inside of the integrated circuit. The coating is for instance a ceramic layer with embedded particles that is provided with a sol-gel processing. The security coating could be applied on top of the integrated circuit, on top of the capacitor, or on both sides. It is understood that it is for this embodiment not absolutely necessary, that the dielectric material of the vertical capacitor is the same as that of the isolation in the vertical interconnect.

Further embodiments are suitable to improve the characteristics of the electronic device. The substrate may comprise a high-ohmic zone which is present adjacent to the vertical capacitors and acts as a protection against parasitic currents. Such high-ohmic zone could circumfere the vertical capacitors and preferably extends from the first to the second side of the substrate. Under 'high-ohmic' is usually understood a zone of more than 500 Ω/ , preferably more than 1500 Ω/ . Such a zone acts as a barrier against any kind of interaction through the substrate. This is particularly advantageous for the reduction of inductive interaction.

In addition to the vertical capacitors, a planar capacitor may be present at the first side of the substrate. Whereas the vertical capacitor generally has a capacitance density in the order of 30 nF/mm^2 or more, a planar capacitor with the same dielectric material has a capacitance density of in the order of 1-5 nF/mm^2. This allows a further fine-tuning of the

desired capacitance. The presence of such capacitors furthermore allows that the electronic device can be applied for more than one application without substantial redesign.

It will be understood by the skilled person that many other elements can be present either on the first side and/or on the second side of the substrate. This includes both active and passive devices, wherein the actives are generally provided in the substrate and the passives are provided on top of the substrate. Also protective layers or specific packages may be provided. In order to cope with differences in thermal expansion between the device and any carrier such as a printed circuit board, an underfill or protective layer such as benzocyclobutene could be provided at the side to be attached to the carrier.

It is a further option that certain semiconductor devices are assembled in a cavity in the substrate. Their backside could be exposed to a heatsink by local removal of the substrate. Such local removal of the substrate can be realized in the same step as the etching from the second side to provide or to open the vertical interconnect. A more detailed description of such a process is given in the non-prepublished patent application EP03101729.6 (PHNL030659), which is herein included by reference. This allows that devices with different substrate materials can be combined with a single interconnect structure, that does not need the provision of any bond wires or solder balls. This has a functional advantage for RF applications in addition to the practical advantage of reduced assembly activities.

It is desired that the device of the invention is assembled together with a semiconductor device into an assembly. The semiconductor device will be attached to either the first side or the second side of the substrate. In order to contact the device, use can be made of a flip-chip process or of wirebonding or optionally of another surface mount technique. A flip-chip process is herein preferred in view of the lower impedance. The solder or metal bumps for the flip-chip process can be chosen corresponding to available processes as well as the desired pitch. The semiconductor device can thereafter be overmoulded with a protective layer. Alternatively a heat-spreader could be provided at the side facing away from the substrate. Instead of one more semiconductor and other electronic devices can be provided at the chosen side of the substrate. Examples of suitable semiconductor devices include devices that need a decoupling capacitor for adequate functioning, such as a power amplifier, a transceiver IC, a voltage controlled oscillator. The further electronic devices may be devices that cooperate with the semiconductor device to provide a functional subsystem. Examples hereof are ESD/EMI protection devices, bandpassfilters, as for instance BAW filters, impedance matching circuits.

The assembly is furthermore suitable for digital signal processing. In such an assembly, the semiconductor device is a microprocessor with an integrated or separate memory unit. Furthermore, a power supply signal generator is provided. The vertical capacitor herein has the function of buffering of the digital signal processing, that is both for decoupling purposes and for dampening power overshoot or drop.

The invention also relates to a method of manufacturing the device of the invention, and particularly to a method of manufacturing an electronic device comprising a semiconductor substrate having a first and a second side and provided with a capacitor and a vertical interconnect extending from the first to the second side, at which first side the capacitor is present and at which second side contact pads are present for connection to a carrier.

It is the object of the invention to provide such a method that is fully compatible to semiconductor manufacturing, without the need to provide special materials or extensive processing at the first and the opposed second side.

This object is achieved in that the method comprises the steps of:

- providing first trenches in the substrate including the step of etching from the first side of the substrate;
- providing second trenches in the substrate by etching from one side of the substrate and opening the second trenches by removing material from the opposite side of the substrate;
- providing said first trenches with a conductive surface;
- applying a layer of dielectric material at the substrate, covering at least the first side of the substrate and the inner faces of the first and second trenches; and
- applying electrically conductive material in the first trenches and in the second trenches, which conductive material in the first trenches forms with the layer of dielectric material and the conductive surface the capacitor, and which conductive material in the second trenches forms the vertical interconnects.

The method of the invention leads to vertical capacitors in combination with vertical interconnects. This is achieved in that the trenches of the capacitors are made simultaneously with the trenches of the vertical interconnects. The structure of a substrate with trenches that then is formed is afterwards processed further in an integral way, so as to provide a dielectric layer and conductive material. There is thus made a separation between the provision of the trenches and the provision of thin-film layers and structures on the substrate. This is enabled due to the fact that the second trenches (for the vertical

interconnects) have a diameter at the first side of the substrate that is slightly larger but still comparable to that of the first trenches.

Basically, there are two embodiments of the method; in the first embodiment the process starts with the simultaneous formation of the first trenches and the second trenches from the first side of the substrate in a single etching process. Thereafter, the second trenches are opened from the second side of the substrate. In the second embodiment, the process starts with the formation of the second trenches from the second side of the substrate; thereafter, the first trenches are formed; if the second trenches do not extend to the first side yet, then this etching step may be used to open the second trenches.

The application of electrically conductive material in the first trenches and the second trenches does not mean that this is the same material, neither that there is a common step in the application of this conductive material for both first and second trenches. It appears advantageous that the conductive material provided in the first trenches forms a seed layer in the second trenches, that is thereafter thickened in an electroplating process. Alternatively, the second trenches, and particularly the narrow part, could be completely filled by the said conductive material, for instance polycrystalline silicon or TiN, TiW or the like. In a further alternative, the second trenches are filled by the provision of a seed only at one of their ends, and subsequent electroplating. Due to the small diameter, that is of the first narrower part of the trenches, they will be filled directly in the plating process. The cavity-like larger part of the second trenches may be filled by electroplating. In the case that this cavity-like parts of the second trenches are provided as a first step, these could be filled with electrically conductive material immediately. Use can be made thereto of various deposition techniques, including sol-gel deposition (for instance of Ag), electroplating, electroless deposition, etc.

It must be understood that the simplification of processes is achieved with the invention, in that the process steps carried out from the second side of the substrate take place at a lower resolution that those at the first side. As a consequence any aligning problems are substantially prevented. Also, the number of steps at the second side appears very limited: basically there are two lithographic steps: one for the provision of an etch mask and one for the definition of a wiring pattern. Particularly wet-chemical etching, wet-chemical deposition and electroplating are in this respect advantageous processes, as a number of substrates can be placed in a bath. It is then not necessary to lie the substrates down at their first side. The etch mask can be provided at the second side of the substrate before any other operation is carried out. Therewith, contamination and damage are prevented. The mask for the definition

of the wiring pattern can be provided after the vertical interconnect is substantially filled, and after that the processing at the first side is substantially completed. The first side is then by preference covered by a protective layer.

These and other aspects of the electronic device, the assembly and the method of the invention will be further elucidated with reference to the figures, in which:

Fig. 1 shows diagramatically a cross-sectional view of a first embodiment of the electronic device;

Fig. 2 a- d show cross-sectional views of four stages in a first embodiment of the method;

Fig. 3 a-e show cross-sectional views of five stages in a second embodiment of the method;

Fig. 4 a-e show cross-sectional views of five stages in a third embodiment of the method;

Fig. 5-7 show different embodiments of the assembly including the device of the invention.

The figures are not drawn to scale and purely diagrammatical. Identical reference numbers in different figures refer to identical parts.

Fig. 1 shows in cross-sectional view a first embodiment of the electronic device 100 of the invention. The device 100 comprises a substrate 10 with a first side 1 and an opposed second side 2. A vertical trench capacitor 20 is present, and exposed at the first side 1, in addition to a vertical interconnect 30. Both the vertical interconnect 30 and the capacitor 20 comprise in this embodiment a plurality of trenches, 21, 311, 312, 313. However, although very much preferred, this is in principle not necessary. The vertical interconnect 30 comprises a first part 31 and a second part 32 of wider dimensions. As will become clear from the further discussion, the first part 31 is made by anisotropic etching from the first side 1, and the second part 32 is made by etching from the second side 2, and particulary wet-chemical etching. The device 100 comprises in at its surfaces at the first and second side 1,2 as well as in the trenches 21, 31, 32 a couple of layers. Not shown here are first conductive surfaces 22, that constitute the bottom electrode of the vertical trench capacitor 20. Shown is a layer 11 of dielectric material, that is present at nearly the complete

surface. On top of the layer 11 of dielectric material, a layer 12 of electrically conductive material is present. This layer is for instance polysilicon, but may alternatively be another material such as copper, sol-gel deposited silver, aluminium.At the first side 1 the capacitor 20 and the interconnect 30 are provided with a further metallisation of AlCu in this case. The layers 12 and 13 can be used as interconnect layers, and may be mutually separated at certain positions by an insulating layer. The second part 32 of the interconnect has its surface covered with a layer 14, in this case of electroplated copper. The copper extends at the second side 2 of the substrate and forms the wiring pattern. The layer 14 may fill the second part of the interconnect 30.

Fig. 2 shows in cross-sectional view four stages in a first embodiment of the method. This first embodiment leads to a device 100 of the first embodiment, with minor variations.

Fig 2a shows the first stage of the method, after etching from the first side has taken place. Use is made herein of dry etching. A mask was used with circular opening of 1.5 μm diameter and 3.5 μm spacing in the area of the capacitors, and openings of 10 μm diameter and 14 μm spacing in the area of the vertical interconnect. The mask contained a stack of 1 μm thermal oxide and 1.3 μm photoresist. The dry etching was executed at wafer level, using substrates of 150 mm diameter. The resistivity of the wafers was in the order of 1 to 5 mΩ.cm, with the exception of high-ohmic zones 18,19 in the substrate, that had a resistivity of 1000-1500 Ωcm. The wafers were etched at room temperature in an ASE™ Inductively Coupled Plasma (ICP) reactor of STS. Typical etching conditions were 12 to 16 mTorr pressure and 20 °C chuck temperature, yielding etch rates of around 0.6 μm/min. With this process the macropore structures are characterized by a smooth pore wall with a rounded bottom and a pore depth uniformity of more than 97%. The trenches 21 with a mask opening of 1.5 μm diameter led to a depth of 40 μm and a diameter of 2 μm. The trenches 311,312,313 with a mask opening of 10 μm diameter led to a depth of 200 μm and a diameter of 12 μm. The pore depth is slightly larger than the mask opening due to underetch. Hence, the difference in openings in the mask led to differences in the pore depth, which phenomenon was exploited effectively in the invention.

Fig 2b shows a second stage in this first embodiment of the method. After the etching, the etch mask was removed, and another mask was deposited. Through this mask, for instance a nitride, an implantation step was carried out. This implantation step provided a first conductive surface 22 in the trenches 21. The mask layout was such that also a

conductive surface 42 was provided, to be used as bottom electrode of a planar capacitor. Between the conductive surface 22 and 42 the high-ohmic zone 18 is present, so as to prevent any parasitic currents as much as possible. Furthermore, a pad 23 was defined in connection to the conductive surface 22, so as to enable electrical connection of the first conductive surface 22. Use was made of a P indiffusion from a pre-deposited phosphorous silicate glass layer. The silicate layer was then removed by wet etching in 1% (v/v) HF.

Fig. 2c shows a third stage in this first embodiment of the method. In a first step hereof, the vertical interconnects 30 were opened from the second side 2 of the substrate 10 by wet-chemical etching. This led to the second parts 32 of the interconnects 30. Use was made herein of a KOH etch. Alternative methods for the interconnect opening include power blasting or lasering . A photolithographical mask was thereto provided at the second side of the substrate. It is observed that in the same step saw lanes can be defined at the second side 2 of the substrate 10. This will simplify the separation of the substrate into individual devices, such that other methods than sawing can be used.

After the provision of the second parts 32 a dielectric layer 11 was deposited. The dielectric layer 11 was in this example a nominally 30 nm 'ONO' dielectric layer stack consisting of a thermal oxide (5 nm), LPCVD nitride (20 nm) and an oxide layer (5 nm) deposited by LPCVD TEOS. The layer was deposited without a mask, such that the complete surface of the device was covered with the dielectric layer 11.

In an alternative embodiment, there vertical interconnect 30 is not opened by wet-chemical etching from the second side, but by removal of part of the substrate. This can be done, by grinding and/or chemical-mechanical polishing. The grinding and/or polishing operation is particularly preferred in combination with the filling of the trenches 311-313 with a sacrificial layer, particularly a spin-on-glass material as known per se. This allows to finalize the thin-film structure at the first side 1 of the substrate 10 before opening the vertical interconnect 30, while at the same time the first side 1 constitutes a relatively planar surface. After opening of the vertical interconnect 30 from the second side, the spin-on-glass material can be removed in a gentle etching treatment, and both the first part 31 and the second part 32 of the interconnect 30 as far as present can be filled with electrically conductive material.

Fig. 2d shows the device 100 after that in the following steps the dielectric layer 11 is partially etched away, and a layer of electrically conductive matrial is provided to define a top electrode 44 of the planar capacitor 40, the second conductive surface 24 of the vertical capacitor 20, the contact 25 to the first conductive surface 23, and the filling of the first part 31 of the vertical interconnect 30. In this example, use is made of a 0.5 μm thick conductive

layer of n-type in situ doped polysilicon. It was deposited by LPCVD from SiH_4 and diluted PH_3. After a furnace anneal step of 30 minutes at 1000 °C the conductivity of the polysilicon is in the order of 1 mΩ.cm. Due to the use of parallel trenches 311, 312, 313 for the first part 31 of the vertical interconnect 30, this conductivity does not lead to an impedance that is too high. The trenches 311, 312, 313 are filled. In this filling process the polysilicon is first deposited at the side-walls and then grows in the kinetic regime. Although not explicitly shown, the polysilicon layer 11 is also used as seed layer for the wiring pattern at the second side 2 of the substrate. This wiring pattern is grown by electroplating thereafter. Alternatively, use can be made of the polysilicon as seed layer also in the first part 31 of the interconnect 30. The trenches 311, 312, 313 in the first part will be completely filled, even if the seed material is present only at their ends.

Instead of the stack of oxide, nitride and oxide, other materials or combinations thereof may be applied as the dielectric material. Such a material can be any single layer of oxide, nitride or the like; any material with a higher dielectric constant, such as tantalum oxide or hafnium oxide, or the like. These layers can be suitably applied with (low pressure) chemical vapour deposition. With this technique, the complete surface as far as uncovered with a mask, is provided with the desired material. An alternative is the use of wet-chemical deposition techniques, including sol-gel processing. It is preferred to apply an oxide layer, such as a thermal oxide, onto the substrate, in order to improve the adhesion. Another alternative is the use of a single nitride layer of about 15 nm – instead of the stack with 30 nm thickness. This increases the capacitance density from 30 to 90 nF/mm^2, but reduces the breakdown voltage from 25 to 7 V.

Fig. 3 shows in cross-sectional view five stages in a second embodiment of the method of the invention. Contrarily to the first embodiment, the first step of the method is herein the provision of the second parts 32 of the interconnects 30 from the second side of the substrate 10. This has the major advantage that after this first step no photolithographical step is needed anymore at the second side 2 of the substrate, until the provision of the wiring pattern 14 in the last step of the method. For reasons of clarity, the trenches 21 of the vertical capacitor are not indicated in this Figure.

Fig. 3a shows the obtained structure after providing the second parts 32 of the interconnect 30 from the second side 2 of the substrate 10. In this case, this was carried out by first providing a mask 51 of oxide and nitride at all sides of the substrates 10, then patterning the mask 51 according to the desired pattern at the second side 2 of the substrate 10 and finally wet-chemical etching of the silicon substrate 10 with KOH.

Fig. 3b shows the result at a second stage of the method. In this method, the the mask 51, or at least the nitride layer thereof, is patterned from the first side 1 of the substrate 10, and used for definition of high ohmic substrate zones (not-shown). Thereafter, a hard mask 52 is deposited and patterned at the first side 1 of the substrate 10 to define the first part 31 of the interconnect 30.

Fig. 3c shows the result at a third stage of the method. First the substrate 10 is etched from the first side 1 through the deposited mask. This etching can be done both with dry-etching and with wet-chemical etching. The etching is preferably carried out in the same step as the etching of trenches 21 to define a vertical capacitor. However, this is not essential. Thereafter, a conductive surface is provided in the manner described earlier with respect to the first embodiment of the method. Only hereafter, the mask 51 is removed, and the dielectric layer 11 is provided without a mask. Thereafter, a layer 12 of electrically conductive material, in this example polysilicon, is deposited and etched in accordance with any desired pattern.

Fig. 3d shows the result at a fourth stage of the method. Contact windows have been etched in the dielectrical layer 11 at the first side 1 of the substrate 10. A thick dielectric layer 15, in this case TEOS, was deposited in part of the windows. Afterwards, a patterned layer 13 of metal has been deposited, while leaving the area of the TEOS layer free.

Fig. 3e shows the result at a fifth stage, after further steps. After provision of a patterned layer 16 of electrically insulating material, a patterned layer 17 of electrically conductive material was provided. This second patterned layer 17, for instance of AlSiCu, has a sufficient thickness, for instance in the order of 1-4 microns, for definition of high-quality inductors. The pattern of electrically insulating material of the layers 15,16 functions as a mechanical support, such that the overlying area in the second metal layer 13 can be used as bond pad 28. The complete structure is then covered with a passivation layer 29, for instance of silicon nitride, that will be locally removed at the area of the bond pad 28. The substrate 10 is thereafter thinned by grinding from the second side 2 thereof. This is of course by no means a necessary step.

Fig. 4 shows cross-sectional views of five stages in a third embodiment of the method of the invention. According to this method, the first side 1 of the substrate 10 is provided with vertical capacitors 20, whereas a semiconductor device 50 is defined at the second side 2 of the substrate.

Fig. 4a shows the first stage of the method. It starts therewith that the semiconductor device 50, for instance an integrated circuit, has been fully processed. The

substrate 10 is thereto a n-type substrate provided at its second side 2 with a p-type epitaxial layer, in which p-well have been defined that act as channels for the individual transistors. An n^+-connection is made from the second side 2 to the n-type substrate layer. This substrate layer has preferably a thickness of more than 40 μm and more preferably a thickness of at least than 70 μm. The n-type layer is at its second side provided with an n^+-layer, so as to enable the effective etching of the vertical capacitors. The second side 2 of the substrate 10 is hereafter protected by a temporary carrier. This could be a glass layer that is attached with a UV releasable adhesive. However, alternatively, it can be a two-layered stack of for instance an 1 micron thick oxide layer and a 1-10 micron thick photoresist layer. This stack can be present at all sides of the substrate 10, as is shown in Fig. 1a. This temporary carrier has the function to withstand pressure differences needed for dry etching, or to define the conditions for wet-chemical etching. The etching mask is furthermore applied to provide the desired implantation step, so as to create the first conductive surfaces of the vertical trench capacitors.

Fig. 4b shows the result after the provision of the first and second trenches 21, 31. Due to the differences in pitch, the depth of the pores is controlled.

Fig. 4c shows the result after removing of the etch mask and after provision of the dielectric layer 11. The removal of the etch mask effectively provides the opening of the second trenches 21 into vertical interconnects 30. The dielectric layer 11 is provided both in the first trenches 21 and in the second trenches 12, and is used as dielectric of the vertical capacitor 20 and as isolation of the vertical interconnect 20. In view of the fully processed integrated circuit, no thermal oxide is used as part of the dielectric layer. Instead, an LPCVD oxide layer is applied. This LPCVD oxide is hereafter locally removed so as to open the bondpads of the integrated circuit 50.

Fig 4d shows the result after the provision of the second electrically conductive surface 12, which is in this case a layer of TiN. This layer 12 is herein used as a seed layer. Alternative deposition techniques for seed layers, such as sol-gel deposition of conductive oxides or sol-gel deposition of Ag.

Fig. 4e shows the result after electroplating. Use is made of a mask, so as to define the desired wiring pattern. A further electrically conductive layer 13 is provided in the trenches 21,31. Thereafter, the parts of the seed layer under the mask are removed. The resulting device is very suitable for integration in a smartcard.

Fig. 5 , 6 and 7 show in diagrammatical cross-sectional view three examples of the assembly according to the invention. Fig. 5 shows an assembly 300 including the device

100, a leadframe 310 and a semiconductor device 200. The assembly makes use of a double flip chip construction, in which the semiconductor device 200 is electrically connected to the leadframe 310 via the electronic device 100. The bumps 201 between devices 100 and 200 are herein for instance gold bumps, and the bumps 301 between leads 311 of the leadframe 310 and the device 100 are for instance solder bumps of SAC (tin-silver-copper alloy). Thermally, the semiconductor device 200 is coupled to the heatsink 312 of the leadframe 310 directly.

This system is assembled in the following manner. Metal has been applied at the bond pad areas of both the device 100 and the active device 200. The device 100 is thereto provided with an underfill metal, such as a Ni or TiW layer on top of the bond pads. The metal is joined in a thermal compression treatment. Thereafter an underfill material is provided so as to fill the area between the device 100 and the active device 200. This underfill acts as a protective layer against moisture and other chemical contamination. layer, which layer is known per se. The leadframe 210 comprises a first and a second electrically conductive layer of Cu. The lead frame 210 is formed by skillfully etching it with a semi-etching technique, first from the first side and then from the second side or the other way around. This results in a heat sink 312 and in leads 311, while the heat sink 312 is also a contact surface. The heat sink 312 is customarily connected to the rest of the lead frame 310 by means of four wires. There is an open space under the leads 311, which is filled with a moulding material. This provides a mechanical anchoring of the leadframe in the moulding material. On the heatsink 312 a conductive adhesive is applied i.e. a silver containing glass epoxy adhesive. Solder dots are provided on the leads 311, for example, by printing with a stencil. The solder is here a low-melting SAC solder which contains over 96% Sn, 3% Ag and about 0.5% Cu.

In an example, the active device 200 together with the bumps 201 then has a thickness of 150 ± 15 μm. The layers of the lead frame 310 have a thickness of 70 ± 20 μm while in the location of the heat sink 312 relative to the device 100 there is a play of about 20 μm. The maximum spreading is thus about 55 μm. This spreading can be eliminated by remelting the solder balls and the solder dots, and slightly in the adhesive layer which, however, is chosen to be thin, for example of a thickness of about 20 μm. After the curing of the conductive adhesive, as a result of a heat treatment of 100-150 °C, the heat sink 312 of the lead frame 310 is then pulled up when the adhesive layer shrinks. The result is a downward pressure. The resulting stress is relaxated by taking the bumps 201, 301 to beyond

their reflow temperature. In this manner the bumps 201,301 are able to distort, and are particularly flattened.

Contrary to the other embodiments, the second side 2 of the device 100 is here not provided with contact pads for coupling to an external carrier. The vertical interconnects 30 provide in this construction a thermal path to the second side 2 of the electronic device 100. This improves the heat-spreading function of the device 100. Although not indicated, it is preferable to provide a connection from the second side 2 of the device 100 to the leadframe 310. Alternatively or additionally, the vertical interconnects 30 are used for grounding. Although two vertical interconnects 30 provide an additional resistance to the ground, this construction of the grounding has the advantage that the ground can be assumed to have the same potential everywhere in the device. Such well defined ground is particularly preferred if the assembly 300 comprises more than a single element. The vertical capacitors (not-shown) are herein provided at the side 1 of the device 100 facing the semiconductor device 200.

Fig. 6 shows an alternative embodiment of the assembly 300. This embodiment has practical advantages for multichip modules, in which more than one device 200 is assembled to the electronic device 100. This electronic device 100 acts here as the carrier of the assembly 300. The advantages are that devices 200 of different height can be included, and that there is no need for a simultaneous attachment of the devices 200 to an individual heatsinks 312 or one common heatsink 312. In addition, the assembly 300 of this embodiment is a chip-scale package without a leadframe, which can be provided at wafer level instead of at die level. Herewith a substantial cost reduction is achieved. A disadvantage of the embodiment is however, the reduced possibilities for thermal dissipation. Although not shown, it is thereto preferred that the heatsink 180 at the second side of the device 100 is provided with solder balls or other means for thermal coupling to an external carrier.

Fig. 7 shows a further embodiment of the assembly 300. This embodiment is a more advanced version of the embodiment of figure 6. It has the further feature that devices 200 are attached to both the first side 1 and the second side 2 of the device 100. If desired, a leadframe with heatsink could be used as shown in Fig. 5.

CLAIMS:

1. Electronic device comprising a semiconductor substrate having a first and a second side and provided with a capacitor and a vertical interconnect through the substrate extending from the first to the second side, at which first side the capacitor is present, characterized in that the capacitor is a vertical trench capacitor provided with a plurality of trenches in which a layer of dielectric material is present between a first and a second conductive surface, said layer of dielectric material is also being used as isolation between the substrate and the vertical interconnect.

2. Electronic device as claimed in Claim 1, wherein the vertical interconnect has a first part and a second part, which first part is exposed at the first side of the substrate, is narrower than the second part and has a substantially cylindrical shape.

3. Electronic device as claimed in Claim 1, characterized in that the trenches of the vertical interconnect are substantially filled with electrically conductive material.

4. Electronic device as claimed in Claim 2, characterized in that the vertical interconnect comprises a plurality of parallel through-holes through the substrate, each of which is filled with electrically conductive material.

5. Electronic device as claimed in Claim 1, characterized in that:
- contact pads for coupling to an external carrier are present at the second side;
- a first vertical interconnect is used for grounding and
- a second interconnect is used for signal transmission.

6. Electronic device as claimed in Claim 4, characterized in that the first and second vertical interconnect are designed so as to form a coaxial structure.

7. Electronic device as claimed in Claim 1, characterized in that an integrated circuit is defined at the second side of the substrate.

8. Electronic device as claimed in Claim 1, characterized in that the substrate comprises a high-ohmic zone which is present adjacent to the vertical capacitors and acts as a protection against parasitic currents.

9. Electronic device as claimed in Claim 1, characterized in that a planar capacitor is present at the first side of the substrate, which planar capacitor comprises the same layer of dielectric material as the vertical capacitor.

10. Assembly comprising the electronic device of any of the preceding Claims, and a semiconductor device, which semiconductor device is electrically connected to bond pads present at the first side of the substrate.

11. A method of manufacturing of an electronic device comprising a semiconductor substrate having a first and a second side and provided with a capacitor and a vertical interconnect extending from the first to the second side, at which first side the capacitor is present, said method comprising the steps of:

- providing first trenches in the substrate including the step of etching from the first side of the substrate;
- providing second trenches in the substrate by etching from one side of the substrate and opening the second trenches by removing material from the opposite side of the substrate;
- providing said first trenches with a conductive surface;
- applying a layer of dielectric material at the substrate, covering at least the first side of the substrate and the inner faces of the first and second trenches; and
- applying electrically conductive material in the first trenches and in the second trenches, which conductive material of the first trenches forms with the layer of dielectric material and the conductive surface the capacitor, and which conductive material of the second trenches forms the vertical interconnects.

12. A method as claimed in Claim 11, wherein the first trenches and the second trenches are etched in a single step, said first trenches having a smaller diameter than the second trenches leading to the through-holes, with the result that the second trenches will extend further into the substrate than the first trenches, said trenches having inner faces.

13. A method as claimed in Claim 12, characterized in that the step of applying conductive material in the second trenches comprises the steps of applying a seed layer and electroplating.

14. A method as claimed in Claim 12, characterized in that a plurality of second trenches are neighbouring and mutually interconnected so as to form a single vertical interconnect.

15. A method as claimed in Claim 14, wherein the electrically conductive material applied in the first and the second trenches is polysilicon.

16. A method as claimed in Claim 11, wherein the step of removing material for opening the second trenches comprising the step of wet-chemical etching to form a cavity, said cavity having a larger diameter than the second trenches.

17. A method as claimed in Claim 11, wherein the second trenches are formed by wet-chemical etching from the second side of the substrate before provision of the first trenches, said second trenches being shaped as cavities and have a larger diameter than the first trenches.

18. A method as claimed in Claim 17, wherein the second trenches are opened by etching in the same step as the etching of the first trenches.

19. A method as claimed in Claim 17, wherein the second trenches extend up to the first side of the semiconductor substrate and are covered by an etch-stop layer provided at the first side of the substrate.

ABSTRACT:

A semiconductor substrate comprises both vertical interconnects and vertical capacitors with a common dielectric layer. The substrate can be suitably combined with further devices to form an assembly. The substrate can be made in etching treatments including a first step from the one side, and then a second step from the other side of the substrate.

Fig. 1

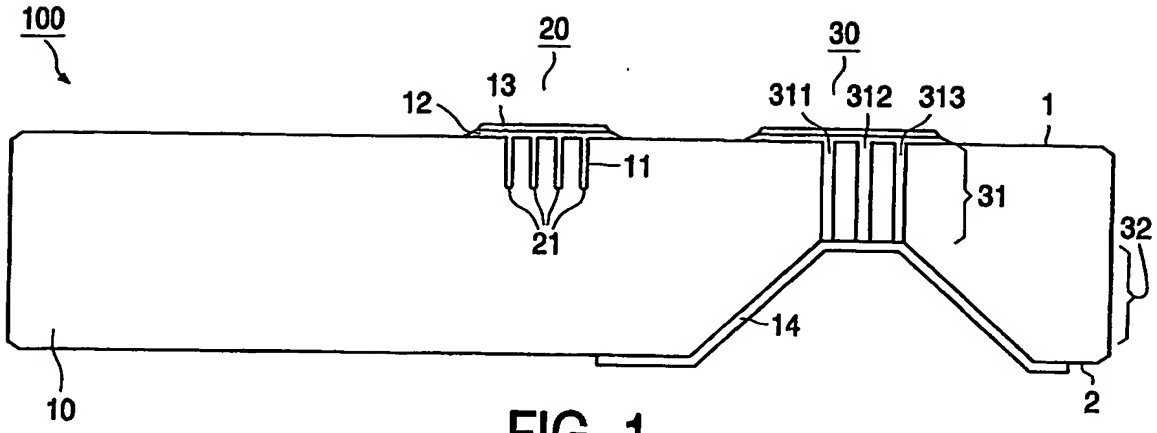

FIG. 1

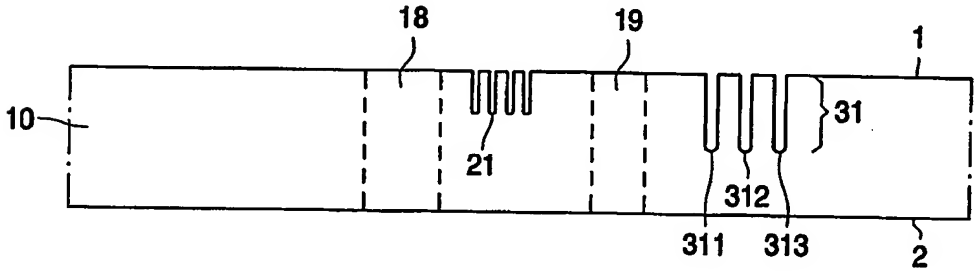

FIG. 2a

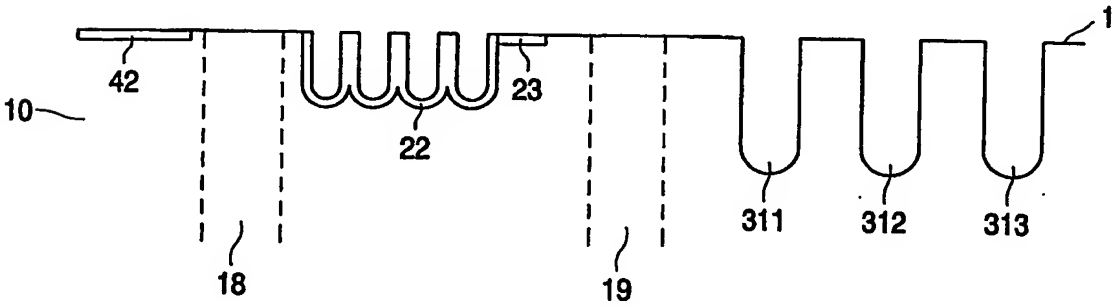

FIG. 2b

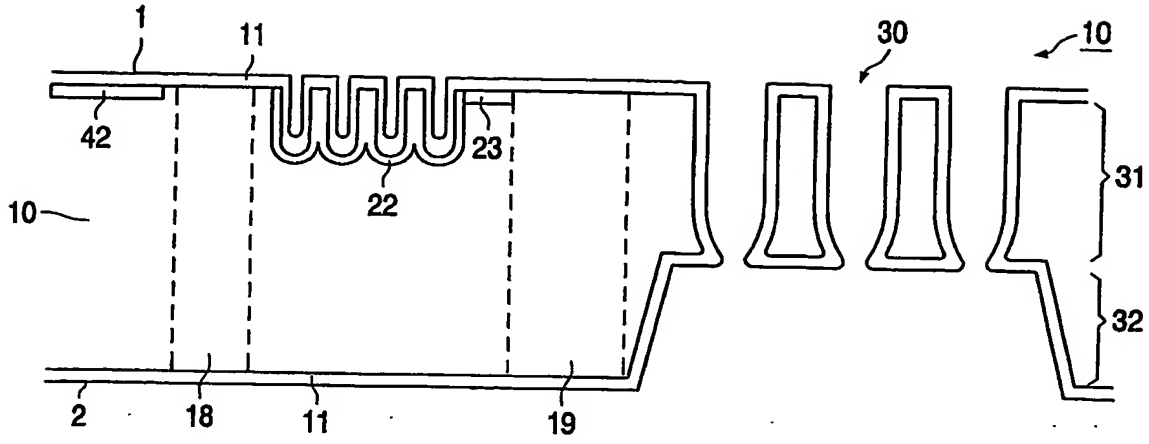
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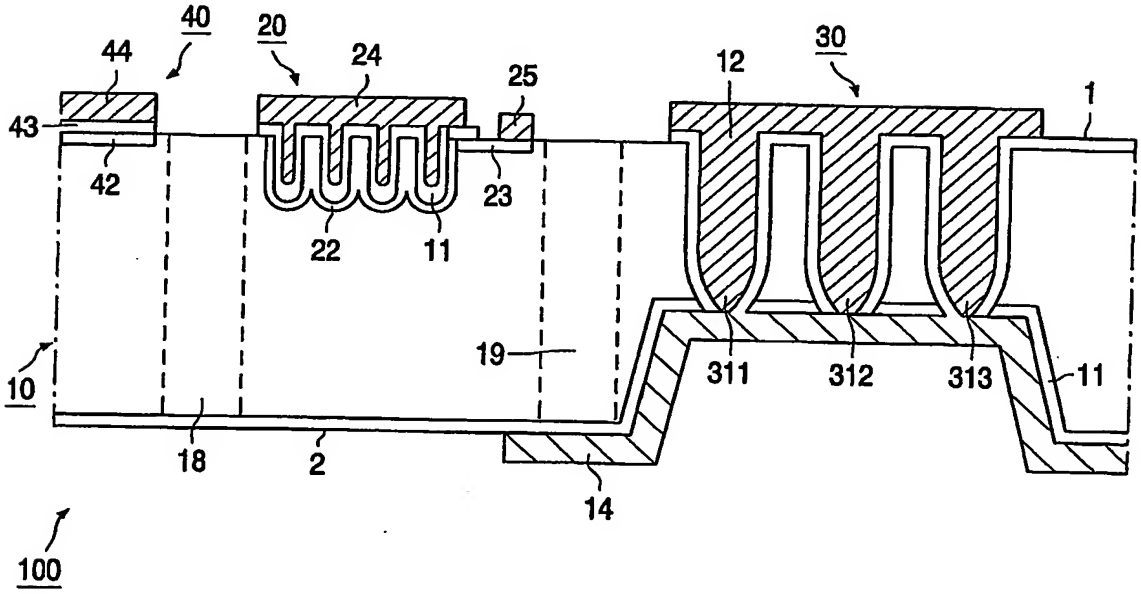
FIG. 2c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312
313
11
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18
2
14
100

FIG. 2d

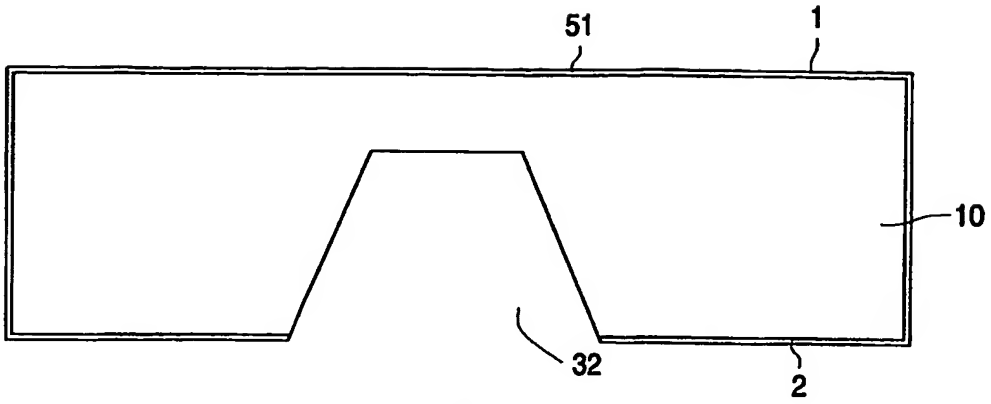

FIG. 3a

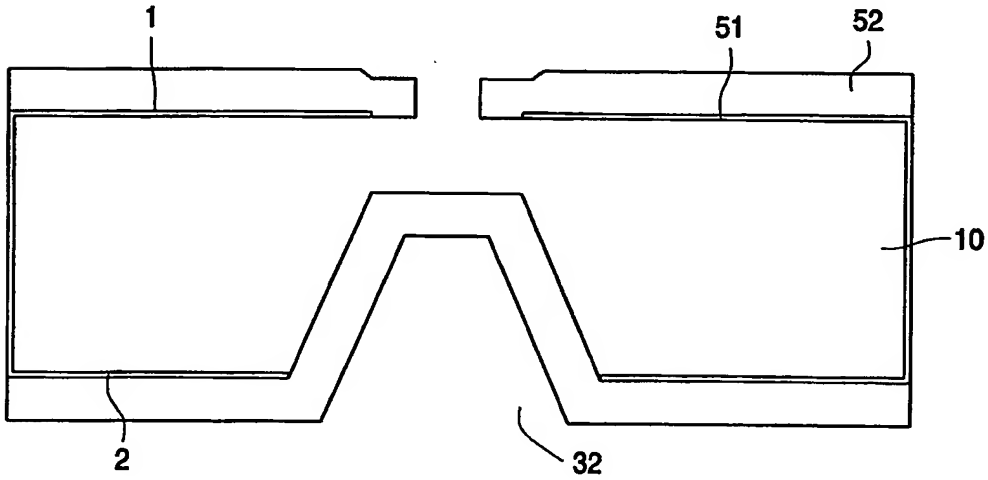

FIG. 3b

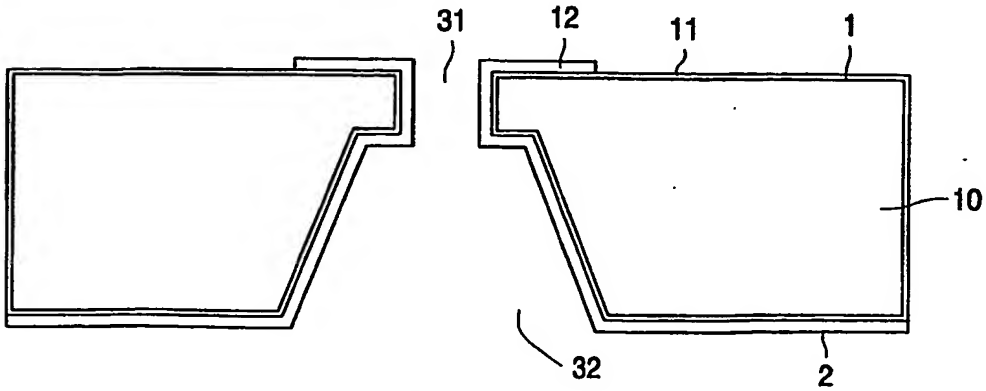

FIG. 3c

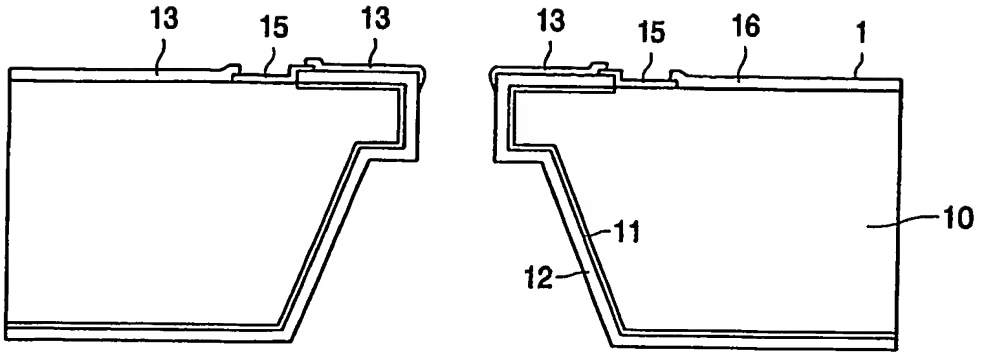

FIG. 3d

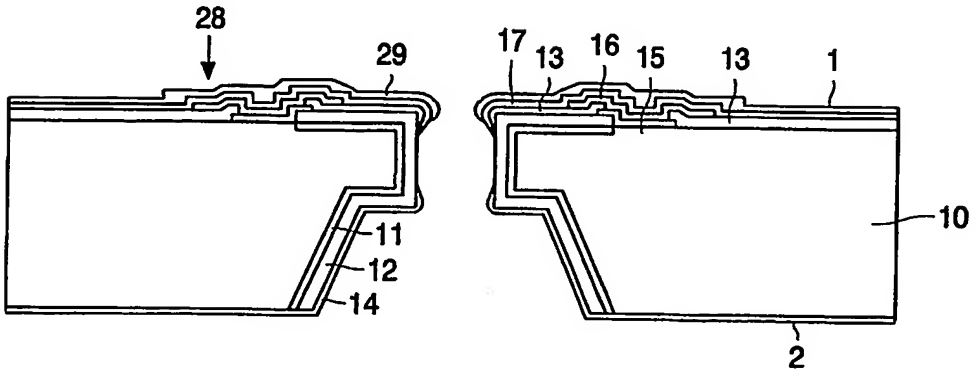

FIG. 3e

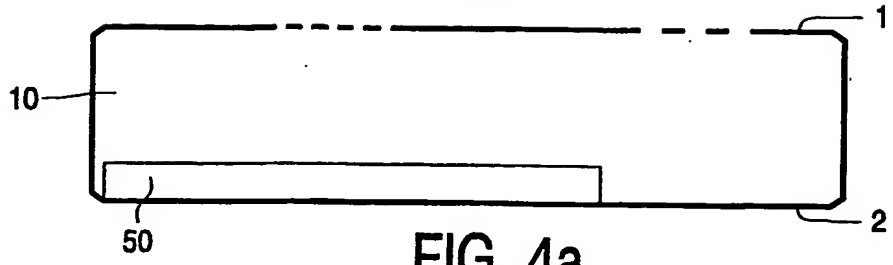

FIG. 4a

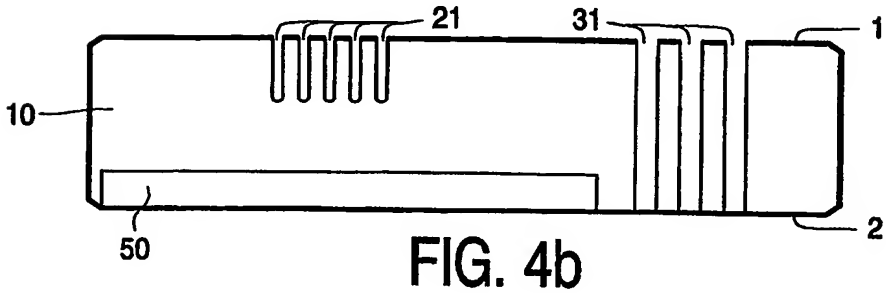

FIG. 4b

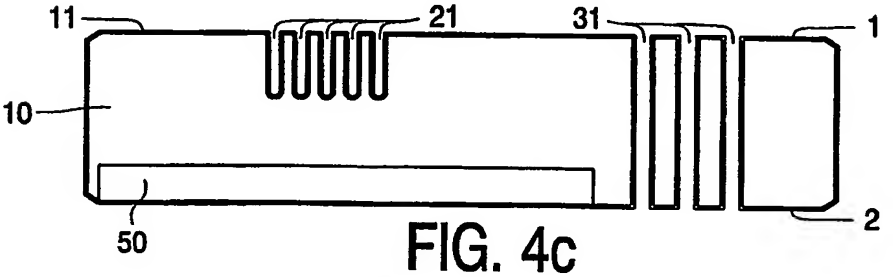

FIG. 4c

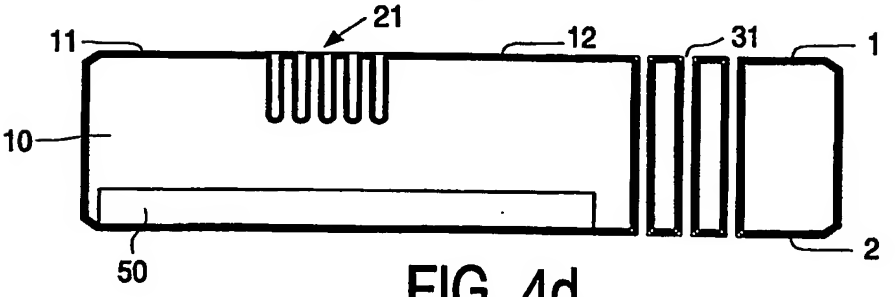

FIG. 4d

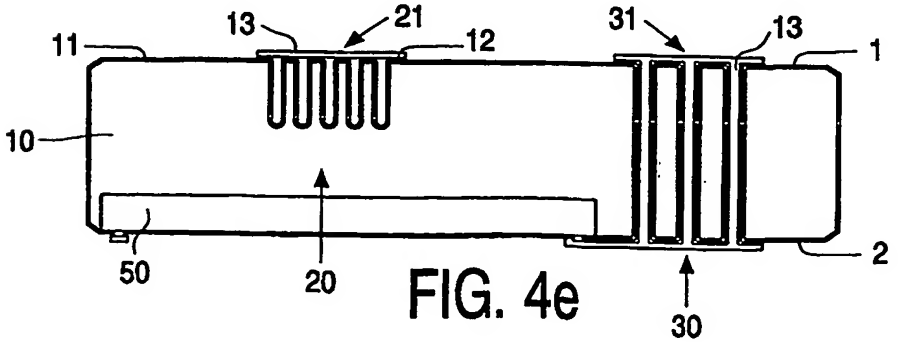

FIG. 4e

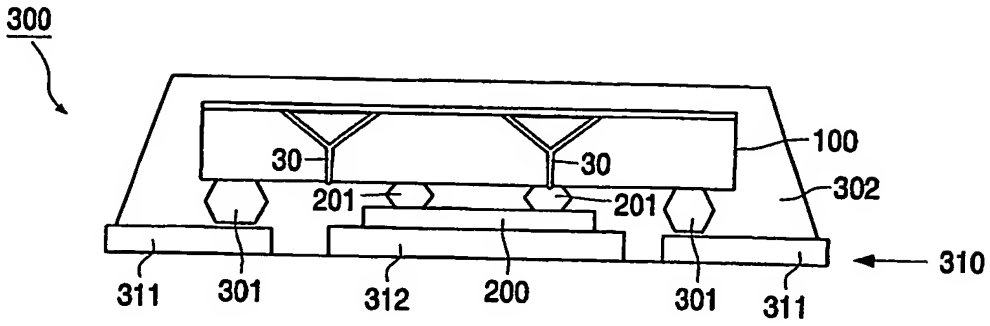

FIG. 5

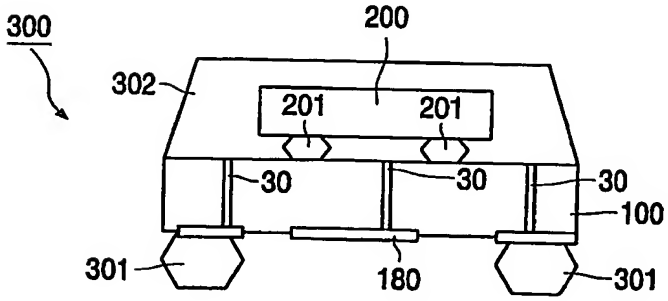

FIG. 6

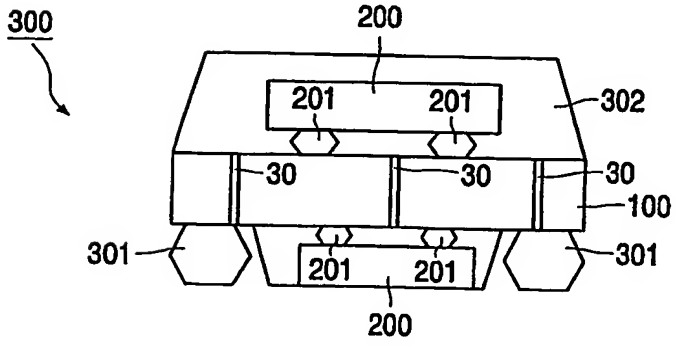

FIG. 7